

Application No.: 09/709,800

Docket No.: JCLA6349

In The Claims:

AI Claim 1. (original) An apparatus for processing data, said apparatus comprising:

a special register bank of N-bit data processing registers;

a general register bank of N-bit data processing registers;

a selector, coupled to the special register bank and the general register bank, for selecting one of the special and general register banks and outputting a selected N-bit result from the selected register bank, wherein the selected N-bit result and a N-bit data form a 2N-bit addition operand;

a multiplier for performing multiply operation upon a first operand and a second operand and outputting an 2N-bit multiplied result;

an accumulator, coupled to the multiplier, the selector and the general register bank, for performing accumulate operation upon the 2N-bit multiplied result and the 2N-bit addition operand and outputting a 2N-bit accumulated result.

Claim 2. (original) The apparatus for processing data of claim 1, wherein the N-bit data is held in the general register bank.

Claim 3. (original) The apparatus for processing data of claim 1, the selector further receiving a class signal, wherein the selector selects one of the special and general register banks in response to the class signal.

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Claim 4. (original) The apparatus for processing data of claim 3, the class signal is used for indicating a first class of instruction or a second class of instruction, wherein the first class of instruction is executing a first calculation of $N*N+2N \rightarrow 2N$ and the second class of instruction is executing a second calculation of $N*N+N \rightarrow N$.

Claim 5. (original) The apparatus for processing data of claim 4, the apparatus further comprising a detecting device, coupled to the accumulator, for receiving the 2N-bit accumulated result and for checking if a case of overflow occurs.

Claim 6. (currently amended) The apparatus for processing data of claim 5, wherein the outputted N-bit result from the selector and the N-bit data held in the general register bank are formed in combination as a first N-bit part and a second N-bit part of the 2N-bit addition operand,

the accumulated result includes a third N-bit part and a fourth~~forth~~ N-bit part,

when the class signal is the second class of instruction, the detecting device comparing the first N-bit part of the 2N-bit addition operand and the third N-bit part of the accumulated result to determine if the case of overflow occurs.

Claim 7. (original) The apparatus for processing data of claim 1, the apparatus further comprising a detecting device, coupled to the accumulator, for receiving the 2N-bit accumulated result and for checking if a case of overflow occurs.

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Claim 8. (currently amended) The apparatus for processing data of claim 7, wherein the outputted N-bit result from the selector and the N-bit data are formed in combination as a first N-bit part and a second N-bit part of the 2N-bit addition operand, the accumulated result includes a third N-bit part and a ~~fourth~~^{fourth} N-bit part, when the class signal is the second class of instruction, the detecting device comparing the first N-bit part of the 2N-bit addition operand and the third N-bit part of the accumulated result to determine if the case of overflow occurs.

Claim 9. (original) A method for processing data using an apparatus having a special register bank of N-bit data processing registers, a general register bank of N-bit data processing registers, a selector, a multiplier and an accumulator, the method comprising:

selecting one of the special and general register banks and outputting a N-bit result from the selected register bank, wherein the N-bit result and a N-bit data form a 2N-bit addition operand;

performing multiply operation upon a first operand and a second operand and outputting an 2N-bit multiplied result;

performing accumulate operation upon the 2N-bit multiplied result and the 2N-bit addition operand and outputting a 2N-bit accumulated result.

Claim 10. (original) The method for processing data of claim 9, wherein the N-bit data is held in the general register bank.

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Claim 11. (original) The method for processing data of claim 10, wherein the step of selecting one of the special and general register banks and outputting N-bit data from the selected register banks further comprising a step of receiving a class signal is determined by a class signal received by the selector.

Claim 12. (original) The method for processing data of claim 11, the class signal is used for indicating a first class of instruction or a second class of instruction, wherein the first class of instruction is executing a first calculation of $N*N+2N \rightarrow 2N$ and the second class of instruction is executing a second calculation of $N*N+N \rightarrow N$.

Claim 13. (original) The method for processing data of claim 12, further comprising a step of receiving the 2N-bit accumulated result and checking if a case of overflow occurs.

Claim 14. (currently amended) The method for processing data of claim 13, wherein the outputted N-bit result from the selector and the N-bit data held in the general register bank are formed in combination as a first N-bit part and a second N-bit part of the 2N-bit addition operand,

the accumulated result includes a third N-bit part and a fourth~~forth~~ N-bit part,

when the class signal is the second class of instruction, comparing the first N-bit part of the 2N-bit addition operand and the third N-bit part of the accumulated result to determine if the case of overflow occurs.

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Claim 15. (original) The method for processing data of claim 9, further comprising a step of receiving the 2N-bit accumulated result and checking if a case of overflow occurs.

Claim 16. (currently amended) The method for processing data of claim 15, wherein the outputted N-bit result from the selector and the N-bit data are formed in combination as a first N-bit part and a second N-bit part of the 2N-bit addition operand, the accumulated result includes a third N-bit part and a fourth~~forth~~ N-bit part, when the class signal is the second class of instruction, comparing the first N-bit part of the 2N-bit addition operand and the third N-bit part of the accumulated result to determine if the case of overflow occurs.
